Short Papers

A 20 GHz Microwave Sampler

K. Madani and C. S. Aitchison

Abstract—**This paper describes a microwave sampler circuit which operates over the frequency band 1–20 GHz and has a number of novel features. These features include a new wideband microstrip to slot balun and a wideband active isolator whose function is to reduce the local oscillator to RF leakage from the input port of the sampler. The signal to noise ratio over the input bandwidth is greater than 20 dB at an input power level of −32 dBm. This signal to noise ratio is measured in an IF bandwidth of 175 MHz and includes the contribution from the IF amplifier. The sampler, which is made on alumina using MIC techniques has an integrated impulse generator which is driven with a sinusoidal local oscillator of only 20 dBm over the frequency band 250–350 MHz. The IF signal is in the band 10–175 MHz. The RF input VSWR is better than 2 : 1 up to 20 GHz whilst the local oscillator to RF breakthrough is better than −58 dBm (−78 dBc) when driven with a local oscillator of 20 dBm. This unusually low leakage has been achieved by using the active isolator prior to the sampling circuit.**

I. Introduction

Microwave samplers are used in microwave frequency counters (1), (2), sampling scopes (3) and other microwave systems and are, therefore, of general interest. They operate in the time domain and are required to have a very wide bandwidth of at least a decade and typically are required to operate up to frequencies of 20 GHz or higher (4), (5). Significant parameters, which it is necessary to satisfy in a good design, are a good RF to IF conversion, a high signal to noise ratio and low switching waveform breakthrough to both the RF input port and the IF circuitry (6). The block diagram of a typical microwave sampler is shown in Fig. 1. It can be seen that it consists of an RF isolator circuit, to which the input analogue signal to be sampled is fed followed by the sampling diode circuit which has incorporated within it an impulse generator and a microstrip to slot line balun. The impulse generator is fed with a sinusoid from an external generator. The sampled signal is fed from the output of the sampling diode to the IF circuitry and the IF amplifier.

The function of the circuit configuration described above is based on the design of a satisfactory sampling circuit using fast Schottky diodes switched by means of an impulse generator based on a step recovery diode. The sampling diode circuit is constructed in a balanced configuration in order to minimise the breakthrough from the step recovery diode impulse generator through the sampling diode circuit. In the design which this paper describes, a further feature is the use of an active isolator circuit which precedes the sampling diode circuit so that impulse power which emerges from the input of the sampling diode circuit is significantly reduced in level by means of the isolator circuit. The function of the IF circuit is to perform matching, shaping and amplification, as well as low pass filtering of the down converted output signal, whilst maintaining an adequate signal to noise ratio.

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K. Madani is with ERA Technology Ltd., Leatherhead, Surrey, KT22 7SA. United Kingdom.

C. S. Aitchison is with the Electrical Engineering Department, Brunel University, Uxbridge, Middlesex, UB8 3PH, United Kingdom.

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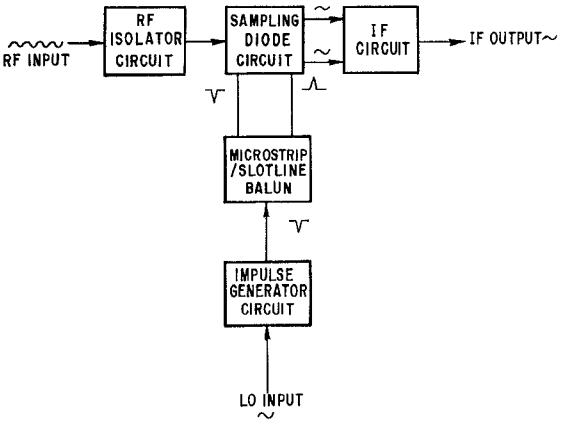

Fig. 1. Block diagram of the sampler system.

II. Sampler Assembly Design

The sampler configuration can be sub-divided into a number of circuit functions. These are listed below:

(a) a balanced sampler with microstrip to slot line balun
(b) an impulse generator
(c) an IF buffer amplifier
(d) an active RF input isolator

Balanced Sampler Design

This consists of a pair of diodes, with sampling capacitors, which are connected across an unbalanced line fed from a generator and terminated in a load. A pair of balanced sampling pulses are fed to the sampling diodes.

The efficiency of a sampling circuit can be expressed as the ratio of the voltage appearing across the sampling capacitor to that of the RF generator whose signal is to be sampled. If the pulse width of the sampling waveform is much longer than the time constant given by the product of the sampling capacitor and the signal source internal resistance, then the sampling capacitor charges to the full value of the input RF voltage and the efficiency approaches unity. This assumes that the capacitor voltage is reset to zero for each new sample. In practice, the beam lead Schottky diodes used as microwave switches have a finite impedance which is generally frequency dependent and the efficiency deteriorates with increasing frequency.

The design of the wideband sampler circuit can be sub-divided into four functional sub-circuits. These are:

(a) the microstrip slot line balun
(b) the Schottky diode sampling circuit
(c) the RF input matching
(d) the IF output matching

1) Microstrip/Slot Line Balun: Of these four circuit blocks, the most significant is the balun since it is necessary that the balun converts the unbalanced impulse produced by the step recovery

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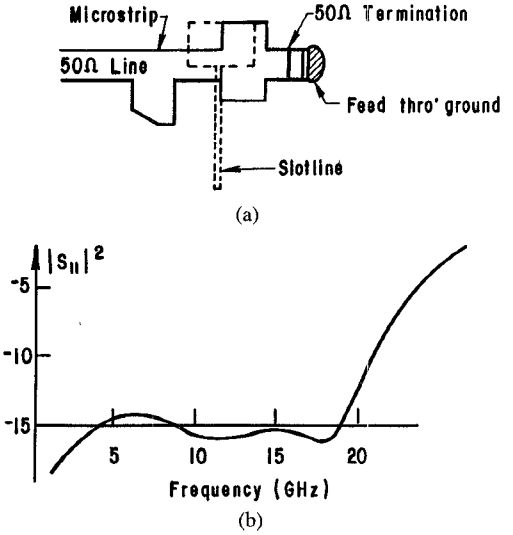

Fig. 2. (a) Arrangement of modified microstrip to slot line configuration. (b) CAD predicted return loss of modified microstrip to slot line configuration.

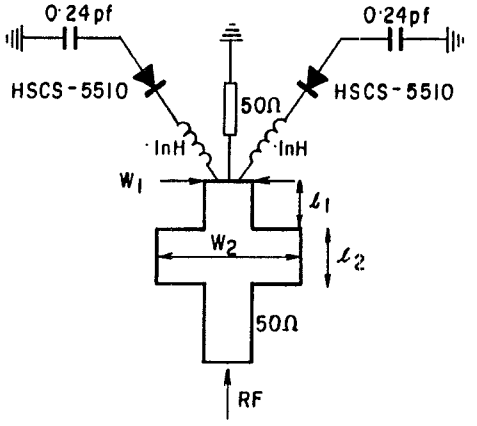

Fig. 3. RF matching circuit, with the RF line connected to the mid point of the sampling diode circuit.

diode to a pair of balanced impulses with opposite polarity. There are a number of ways in which such a balun can be implemented. A convenient choice compatible with planar circuit technology is to use a slot line which would propagate the energy in the odd mode. A microstrip slot line transition can then be used as a balun because the input signal to the microstrip line propagating in the even mode can be picked up as a pair of balanced signals of opposite polarity on either side of the slot line. This design is essentially that of the Marchand balun filter (7), (8) frequently used in wideband applications. In the present sampler circuit, the conventional microstrip/slot line transition has been modified by adding a 50 Ω termination as illustrated in Fig. 2 which results in a 10 dB return loss up to more than 20 GHz as shown. The best way of determining the practical balancing behavior of the transition is in conjunction with the measurement of the sampler.

2) Diode Sampling Circuit: The sampling diodes which were selected are the Hewlett Packard HSCS-5510 beam lead. The sampling capacitors were realized in microstrip as lumped parallel plate capacitors. The maximum value of the capacitance which is achievable on 0.635 mm alumina is 0.27 pF whilst maintaining the constraint that the capacitance behaves as a lumped circuit.

3) RF Matching Circuit: An RF matching circuit is required for a good input match of the RF signal to the sampling diodes. This circuit was designed to be as simple as possible yet to produce a broadband performance. Fig. 3, shows the RF matching circuit which was used for this purpose. The line lengths l_1 and l_2 and line widths, W_1 and W_2 have been optimised so as to obtain satisfactory S_{11} with an acceptable magnitude over the frequency range of interest giving the best return loss possible. The computed return loss was better than 12 dB up to 20 GHz.

4) IF Circuit: The IF output circuit is required to analogue process the IF output in the form of a pair of balanced signals which are taken from the two sampling capacitors. The combined output is fed as a single ended signal to the IF matching network followed by an IF amplification stage.

III. Step Recovery Diode Impulse Generator

The basic step recovery diode generator consists of a step recovery diode device in shunt with a load, the combination of which is fed through a series drive inductance from a sinusoidal generator. During the positive half cycles from the generator, energy is stored in the drive inductance. In the negative half cycles, and when the voltage drops below a threshold value the diode snaps open and the current in the diode falls sharply to zero. Thus the energy stored in the inductance is discharged into the parallel resonant circuit formed by the inductance, the diode capacitance and the load resistor. The width of the resultant impulse is simply half of the period of the natural resonant frequency of the parallel resonant circuit. Significant additional rings are suppressed because the diode turns on every time the ringing cycle goes positive. The impulse generator was designed to operate satisfactorily in the frequency band of 275–350 MHz. A step recovery diode in chip form, together with the π-matching network were mounted on a gold plated chip mount of 2 mm diameter fixed through a hole in the alumina substrate and with 25 micron gold bond wires between pads on the alumina substrate as the inductances. The output impulse measured with a 25 ps rise time sampling oscilloscope shows an uncorrected transition time of about 125 ps. A short circuited slot line with a delay length of 20 ps was provided to reflect back the impulse. With this technique the sampling diodes were first switched on by the rising edge of the impulse, but they were switched off by the reflected edge of the same impulse some 40 ps later.

The return loss of the step recovery diode impulse generator over the input band (275–350 MHz) was measured to be better than 8 dB at an input level of 27 dBm. The frequency domain spectrum showed harmonic content up to 20 GHz, better than −40 dBm.

IV. Active RF Input Isolator

To improve the isolation of the input of the sampler to the switching waveform feedthrough, it was decided to add an isolator at the input of the sampler. No miniature passive component is available for this purpose, thus an active amplifier was used. This consisted of a single stage MESFET using hybrid MIC technology. This amplifier was designed to have a modest gain of about 1 dB over the band 100 MHz-20 GHz, but had an isolation of not less than 30 dB over the same band, together with an input return loss better than 10 dB. The breakthrough at the input of the transient switching waveform was measured to be extremely good at a level of −78 dBc.

V. Sampler Architecture

All the circuits described above were integrated on a single alumina substrate of dimensions 11 mm × 11 mm, with the exception of the active isolator and the IF buffer amplifier. All these

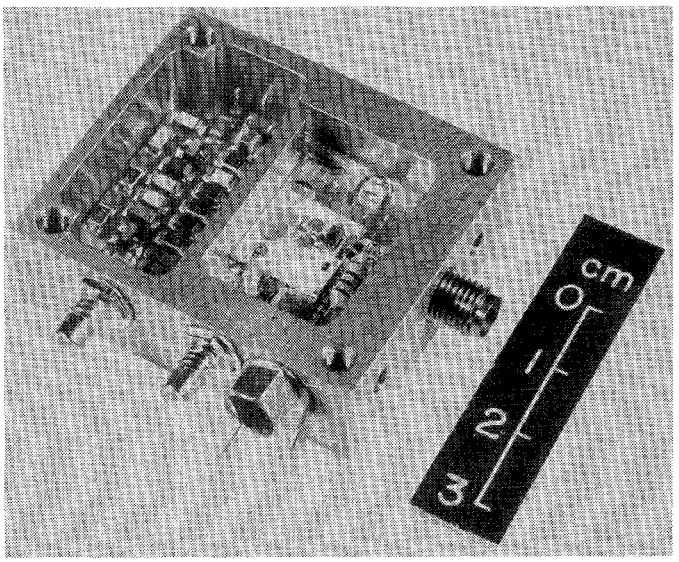

Fig. 4. Sampler assembly housing showing sampler circuit and isolator (right hand side) and IF amplifier (left hand side).

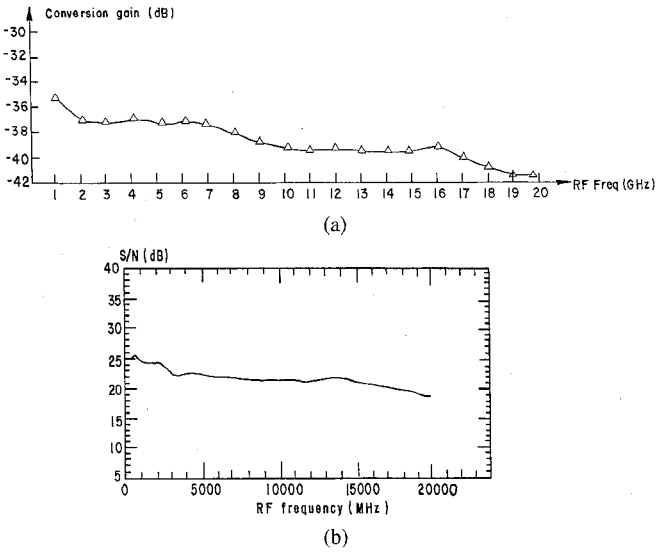

Fig. 5. (a) Measured conversion gains of sampler (without IF amplifier). (b) Measured signal to noise ratio for sampler assembly including IF amplifier (input signal power is −32 dBm and measurement bandwidth is 175 MHz).

TABLE I
SUMMARY OF SAMPLER ASSEMBLY PERFORMANCE

[1]	Frequency band	1–20 GHz
[2]	Input VSWR	≤2 : 1
[3]	RF to IF conversion loss with no IF amplification	+36 dB at 2 GHz +42 dB at 20 GHz
[4]	Signal to noise ratio measured in 175 MHz bandwidth with input signal of −32 dBm	+25 dB at 2 GHz +20 dB at 20 GHz
[5]	Step recovery diode drive power	20 dBm
[6]	Sampling waveform leakage from sampler assembly input port	≤ −78 dBc
[7]	IF output flatness over 10 to 175 MHz	±1 dB
[8]	1 dB output power compression point at 10 GHz input	+6 dBm
[9]	Sampler assembly dimensions mm	40 × 35 × 10 (approx.)

circuits were then housed in an aluminium box with a K-type RF input connector. A photograph of the module is shown in Fig. 4.

VI. The Sampler Performance

The conversion loss of the sampler circuit without the IF amplifier is illustrated in Fig. 5(a) and shows a conversion loss of 36 dB at a frequency of 1 GHz degrading to 42 dB at 20 GHz. The addition of the IF amplifier added an extra 20 dB gain to the sampler at the expense of some reduction in the signal to noise ratio. This measurement was obtained with an IF frequency of 120 MHz, an input signal level of −5 dBm and a local oscillator frequency of 275 MHz at a power level of 20 dBm. The measured output signal to noise of the complete sampler module, including the IF amplifier, as a function of RF frequency is shown in Fig. 5(b). For an input RF signal level of −32 dBm, the signal to noise ratio was measured to be at least 20 dB at 20 GHz in a bandwidth of 175 MHz. The input VSWR was better than 2 to 1 over the total band up to 20 GHz. With a local oscillator frequency of 275 MHz at a power level of 20 dBm, the LO to RF breakthrough was better than −58 dBm (−78 dBc) for each harmonic.

Table I summarizes the measured performance of the sampler module.

VII. Conclusion

A microwave sampler module with some novel features has been designed, constructed and evaluated satisfactorily. With a sinusoidal LO drive level of only 20 dBm and a sampling rate over the band of 250–350 MHz, the sampler gave an excellent signal to noise performance of at least 20 dB when measured in a bandwidth of 175 MHz with a signal input of −32 dBm up to 20 GHz. The conversion loss without the IF amplification was better than 42 dB up to 20 GHz. The switching impulse breakthrough to the RF input port was particularly low at −78 dBc by virtue of the integration of an active isolator stage.

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Characterizing Microwave Planar Circuits Using the Coupled Finite-Boundary Element Method

Ke-Li Wu, Chen Wu and John Litva

***Abstract*—A general approach is presented for the analysis of microwave planar circuits. The technique is particularly well suited to the analysis of circuits with complicated geometries and dielectric loads. The proposed technique is a hybrid, consisting of an amalgamation of the finite element and the boundary element techniques. The new technique can handle problems with mixed electric and magnetic walls, as well as complicated dielectric loads, such as those composed of ferrite materials. Computed and measured data for various complicated devices are compared, showing excellent agreement.**

I. Introduction

In the development of numerical techniques for analyzing the electromagnetic fields associated with microwave circuits, one has to strike a balance between accuracy and simplicity. Three dimensional full-wave analyses are often impractical because they result in long computational times and prohibitively large memories requirements. In contrast, a simple planar waveguide model can be used in the analysis. This model is particularly useful for solving microwave printed circuit problems. Several methods have been used in the past for the analysis of planar circuits. When the circuit pattern is as simple as a square, rectangle, circle, or annular section, field expansion in terms of resonant models can be used. A general procedure of this technique has been described by Okoshi [1]. When using this method, one must start by calculating the eigenfunctions and eigenvalues for the circuit being analyzed. This can be done analytically if the structure is a separable geometry; if the geometry is not separable, the numerical analysis can be carried out using the contour integral representation of the wave equation.

In practice, it is highly desirable for CAD software to have the capability of analyzing arbitrarily shaped planar circuits. The Finite Element Method (FEM) [2] has been used to handle the discontinuities of arbitrarily shaped planar circuits, even though the computational overhead is large. The boundary integral method or Boundary Element Method (BEM) [3] seems to offer the promise of greatly increased efficiency because it reduces the size of planar circuit problems from two-dimensions to one-dimension. However, when the planar circuits involve complicated or anisotropic dielectric loads, the difficulty of the solution increases quite considerably for one-dimensional algorithms.

In this paper, the coupled finite-boundary element method (CFBM), which was originally developed for waveguide discontinuities [4], is adopted for application to general microwave planar circuit structures. The circuits can include electric walls, magnetic walls, and complex dielectric loads. The CFBM has the merits of both the FEM and the BEM, and can be used to solve complicated problems without requiring excessive computer memory and computation time. Using this method, only the complex media subdomains, which may consist of lossy or anisotropic materials, need to be treated using FEM. Elsewhere, the BEM is used on the boundary to take into account the circuit configuration. Comparing the hybrid technique with the FEM (two-dimensional algorithm) and BEM (one-dimensional algorithm), one concludes that the CFBM can be considered to be a one and one-half dimensional algorithm for planar circuit analysis.

The validity of the application of CFBM to the analysis of planar circuits will be demonstrated with various illustrative examples, which include a cavity filter using metallic posts as inductive shunts, a microstrip disk filter with a dielectric load, and a planar ferrite circulator. The numerical results obtained with CFBM are compared with both measured results and published results. The comparisons are shown to be in good agreement.

II. The Planar Circuit Model

There are various techniques that can be used for accurately determining both the equivalent waveguide width $W_{\text{eff}}(f)$ and equivalent filling dielectric constant $\epsilon_{\text{eff}}(f)$. Since they are well known they will not be discussed here for simplicity. When characterizing microstrip or strip line circuits using an equivalent cavity, surrounded by magnetic walls, it is necessary when establishing the equivalent dimensions to take into account the energy stored in the circuit's fringing field. The stored energy can be estimated by assuming that the electric and magnetic fields are constant throughout the increased volume ΔV and are equal to the field at the edge of the circuit. For instance, the increased volume ΔV for a circular disk is taken to be equal to the volume corresponding to the static fringe capacitance ΔC between the radius a and the equivalent radius a_{eq} of the fringe edge, where

$$a_{eq} = a\left\{1 + \frac{d}{\epsilon\pi a^2}\Delta C\right\}^{1/2}, \tag{1}$$

and the static fringe capacitance ΔC can be derived using Kirchhoff 's equation. The equivalent parameters for other geometries can be obtained in a similar way.

It is usually assumed that the equivalent dimensions reflect only the characteristics of the fringing fields when unperturbed by inhomogeneities in the planar circuits, such as a dielectric loads or conductor posts. It can be shown, by comparing the numerical results with the experimental results, that this assumption is fairly reasonable because the equivalent dimensions are determined mostly by the fringing of the outermost fields.

III. General CFBM Formulation for Planar Circuits

The general planar circuit problem shown in Fig. 1 will now be addressed. An M-port device is assumed, where the boundary Γ_Q encloses the inhomogeneous subdomain; boundary Γ_0' is the possible electric wall in the circuit; and the boundary $\Gamma' = \Gamma_0' \cup \Gamma_Q \cup_{m=0}^{M} \Gamma_m$, completely encloses the remaining homogeneous domain.

When using the CFBM technique, complicated subdomains, consisting of dielectric or ferrite posts, can be treated using the

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The authors are with the Communications Research Laboratory, McMaster University, 1280 Main Street West, Hamilton, ON, Canada L8S 4K1.

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